# Lab 07 – Worksheet

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| Name: Ali Muhammmad Asad | ID: 07190 | Section: T6 |

## Selective 2’s complement

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| --- | --- | --- | --- | --- | --- | --- |
| **Inputs to complement** | | | | **Outputs of the complement** | | |
| **O** | **B2** | **B1** | **B0** | **C2** | **C1** | **C0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 |

Write expressions for C2, C1 and C0

Table 7.2

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| --- | --- |
| C2 = | O’B2 + B2B1’B0’ + OB2’B0 + OB2’B1 |
| C1 = | O’B1 + B1B0’ + OB1’B0 |
| C0 = | B0 |

*Provide appropriately commented code for your selective 2’s complement module*

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| `timescale 1ns / 1ps  module complement\_2s(  input [2:0] B,  input O,  output [2:0] C  );  assign C[2] = ~O&B[2] || B[2]&~B[1]&~B[0] || O&~B[2]&B[0] || O&~B[2]&B[1];  assign C[1] = ~O&B[1] || B[1]&~B[0] || O&~B[1]&B[0] ;  assign C[0] = B[0] ;  endmodule |

Write a testbench to thoroughly test designed complement module.

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| `timescale 1ns / 1ps  module testbench\_complement\_2s();  reg[2:0] bB;  reg oO;  wire [2:0] cC;  complement\_2s test(bB, oO, cC);  initial begin  #100 bB = 3'b000; oO = 0;  #100 bB = 3'b001; oO = 0;  #100 bB = 3'b010; oO = 0;  #100 bB = 3'b011; oO = 0;  #100 bB = 3'b101; oO = 0;  #100 bB = 3'b111; oO = 0;  #100 bB = 3'b000; oO = 1;  #100 bB = 3'b001; oO = 1;  #100 bB = 3'b010; oO = 1;  #100 bB = 3'b011; oO = 1;  #100 bB = 3'b101; oO = 1;  #100 bB = 3'b111; oO = 1;  end  endmodule |

*Attach screenshot of Simulation output- make sure to scale properly for visibility of all case.*

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## Adder/Subtractor system

*Provide code for design module here*

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| `timescale 1ns / 1ps  module adder\_subtractor(  input [2:0] A,  input [2:0] B,  input O,  output [6:0] S,  output X  );  wire[2:0] C;  wire[2:0] Sum;  wire[2:0] D;  wire[3:0] sX;  wire carry, E, Y;  complement\_2s c1(B, O, C);  threeBitAdder tba(A, C, Sum, carry);  my\_or or1(~O, carry, X);  and\_gate and1(~O, carry, E);  assign sX = {E, D};  complement\_2s c2(Sum, ~X, D);  segment\_decoder s1(sX, S);  endmodule |

*Add your testbench here*

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| *`timescale 1ns / 1ps*  *module testbench\_adder\_subtractor();*  *reg[2:0] A;*  *reg[2:0] B;*  *reg sbit;*  *wire [6:0] S;*  *wire dp;*  *adder\_subtractor test(A, B, sbit, S, dp);*  *initial begin*  *#100 A = 3'b011; B = 3'b100; sbit = 0; //3 + 4*  *#100 A = 3'b011; B = 3'b100; sbit = 1; //3 - 4*  *#100 A = 3'b111; B = 3'b111; sbit = 0; //7 + 7*  *#100 A = 3'b010; B = 3'b110; sbit = 1; //2 - 6*  *end*  *endmodule* |

*Attach screenshot of waveform results here*

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## Exercise

Use Figure 6.0 and work out for cases when B is zero and subtracted from A. Reflect on the output obtained and suggest ways to fix (if required).

*Space to work out on Figure 7.0*

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*Space for reflection*

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## Lab Evaluation Rubrics

**Marks Distribution:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR10**  **Analysis** |
| **In-lab** | **Task b** | 20 points | 15 points | 10 points | 10 points | - |
| **Task c** | 20 points | - | 10 points | - |
| **Exercise** | **Task d** | - | - | - | 15 Points |
| **Total Marks =** | **100** | 40 | 15 | 20 | 10 | 15 |

**Marks Obtained:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR10**  **Analysis** |
| **In-lab** | **Task b** |  |  |  |  | - |
| **Task c** |  | - |  | - |
| **Exercise** | **Task d** | - | - | - |  |
| **Total Marks =** | **100** |  |  |  |  |  |